This Listing of Claims will replace all prior versions, and listings, of claims in the application:

**LISTING OF CLAIMS:**

1. (Currently Amended) A nonvolatile semiconductor memory device comprising:

a memory array ~~composed of~~ comprising a plurality of floating-gate field-effect ~~transistor~~ transistors ~~connected to a row line and a column line and~~ disposed in a matrix configuration, the transistors being connected to corresponding row lines and column lines, at least one of the transistors comprising ~~the floating-gate field-effect transistor including~~

a source and a drain which are formed inside a P-type well ~~provided~~ formed inside an N-type well formed on a semiconductor substrate,

a floating gate formed [[over]] above a portion of the semiconductor substrate between the source and the drain with an insulating film interposed ~~therebetween~~ between the floating gate and said portion of the semiconductor substrate, and

a control gate formed on the floating gate with [[a]] another insulating film interposed therebetween;

a first voltage application ~~means for~~ circuit applying a first voltage to the P-type well when an erasing pulse is applied; and

a second voltage application ~~means for~~ circuit applying a second voltage to the N-type well when [[an]] the erasing pulse is applied.

2. (Currently Amended) The nonvolatile semiconductor memory device ~~as defined in Claim~~ of claim 1, wherein the first voltage and the second voltage are positive voltages, and the second voltage is higher than the first voltage.

3. (Currently Amended) The nonvolatile semiconductor memory device ~~as defined in Claim~~ of claim 1, wherein the first voltage application ~~means is~~ circuit comprises a first high-voltage pumping circuit for generating the first voltage, and the second voltage application ~~means is~~ circuit comprises a second high-voltage pumping circuit for generating the second voltage.

4. (Currently Amended) The nonvolatile semiconductor memory device ~~as defined in Claim~~ of claim 1, wherein the first voltage application ~~means is~~ circuit comprises a ~~first~~ high-voltage pumping circuit for generating the first voltage, and the second voltage application ~~means is~~ circuit comprises an auxiliary pumping circuit for ~~generating the second voltage higher than~~ raising the first voltage ~~by receiving~~ to generate the ~~first~~ second voltage.

5. (Currently Amended) The nonvolatile semiconductor memory device ~~as defined in Claim~~ of claim 1, wherein the second voltage application ~~means is~~ circuit comprises a high-voltage pumping circuit for generating the second voltage ~~higher than the first voltage~~, and the first voltage application ~~means is~~ circuit comprises a regulator circuit for ~~generating the first voltage lower than~~ lowering the second voltage ~~by receiving~~ to generate the ~~second~~ first voltage.